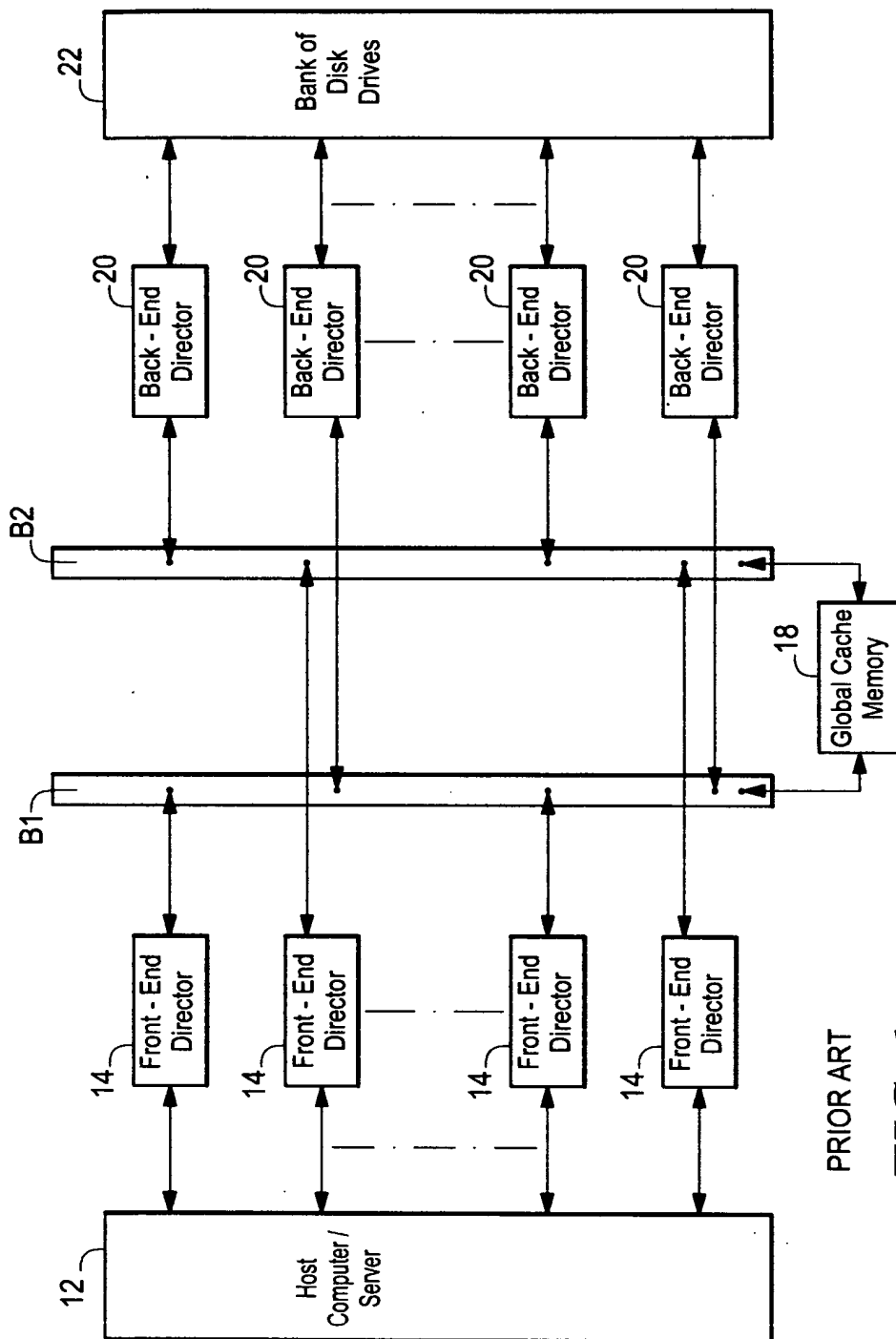


Serial No. 09/680156
Replacement Drawings

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PRIOR ART

FIG. 1

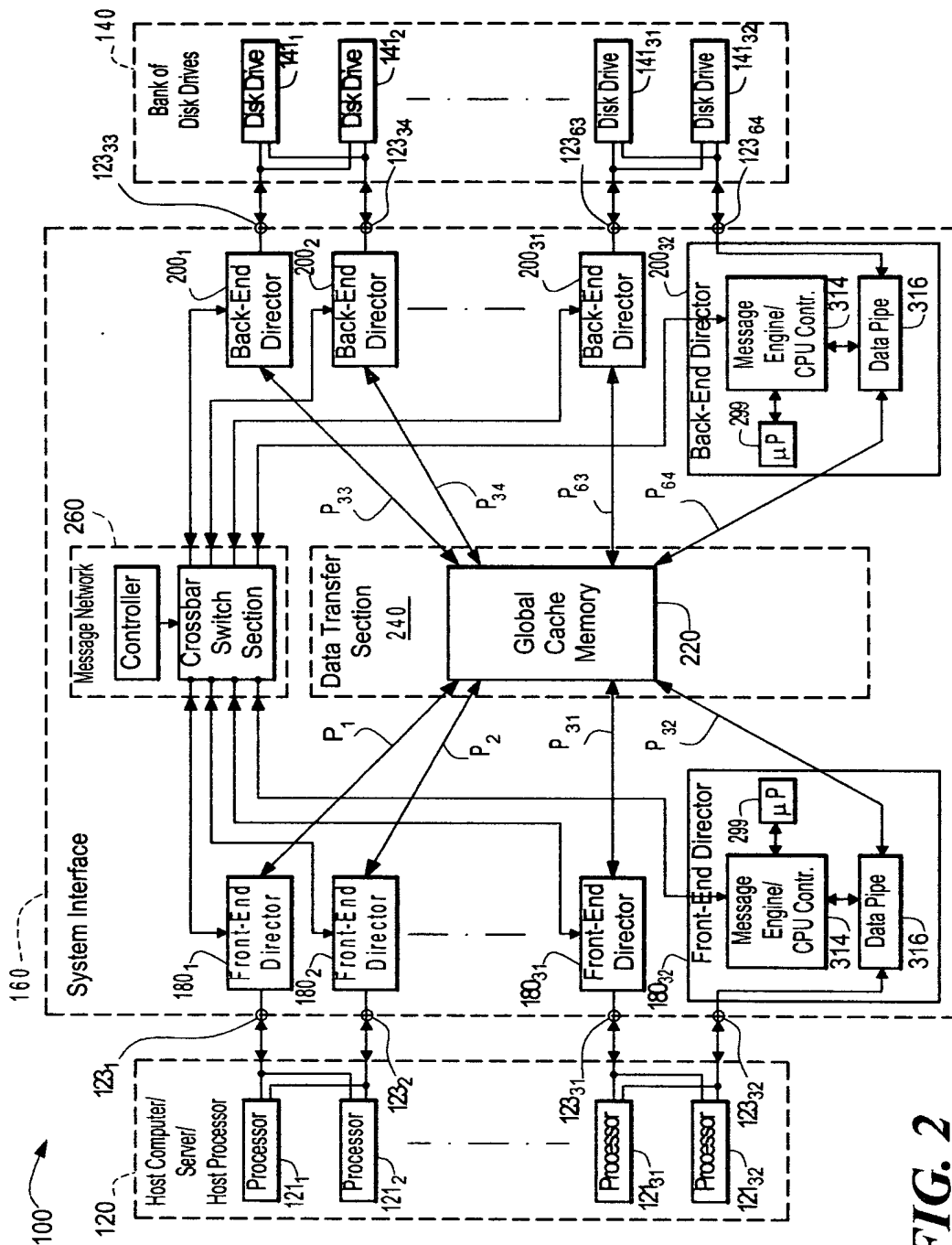
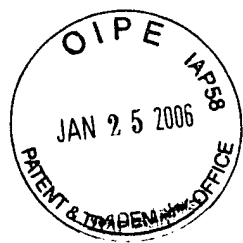


FIG. 2



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FIG. 3

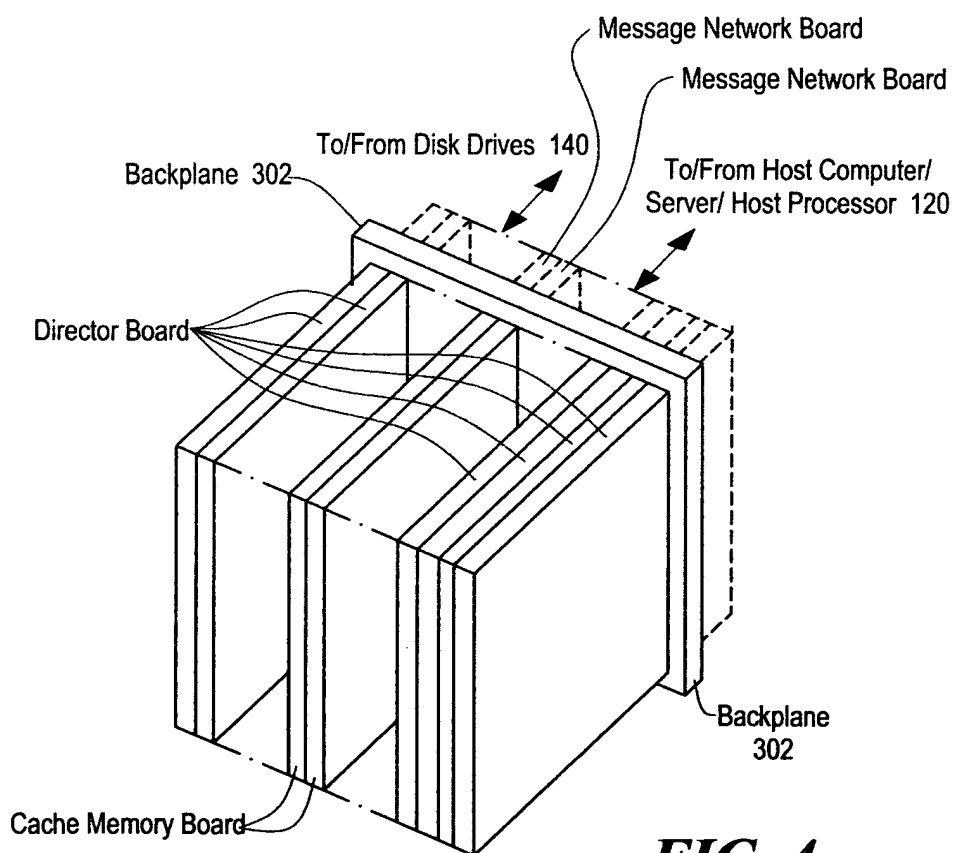
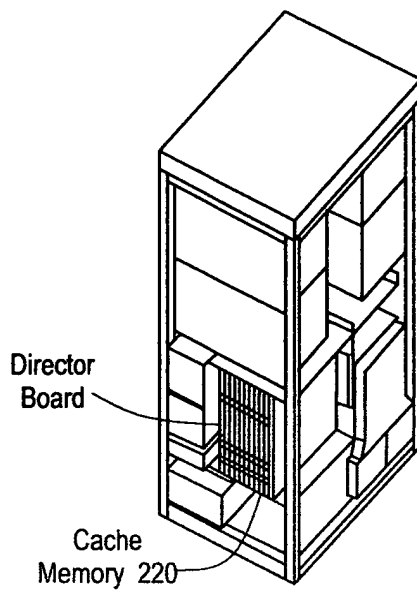


FIG. 4



FIG. 5

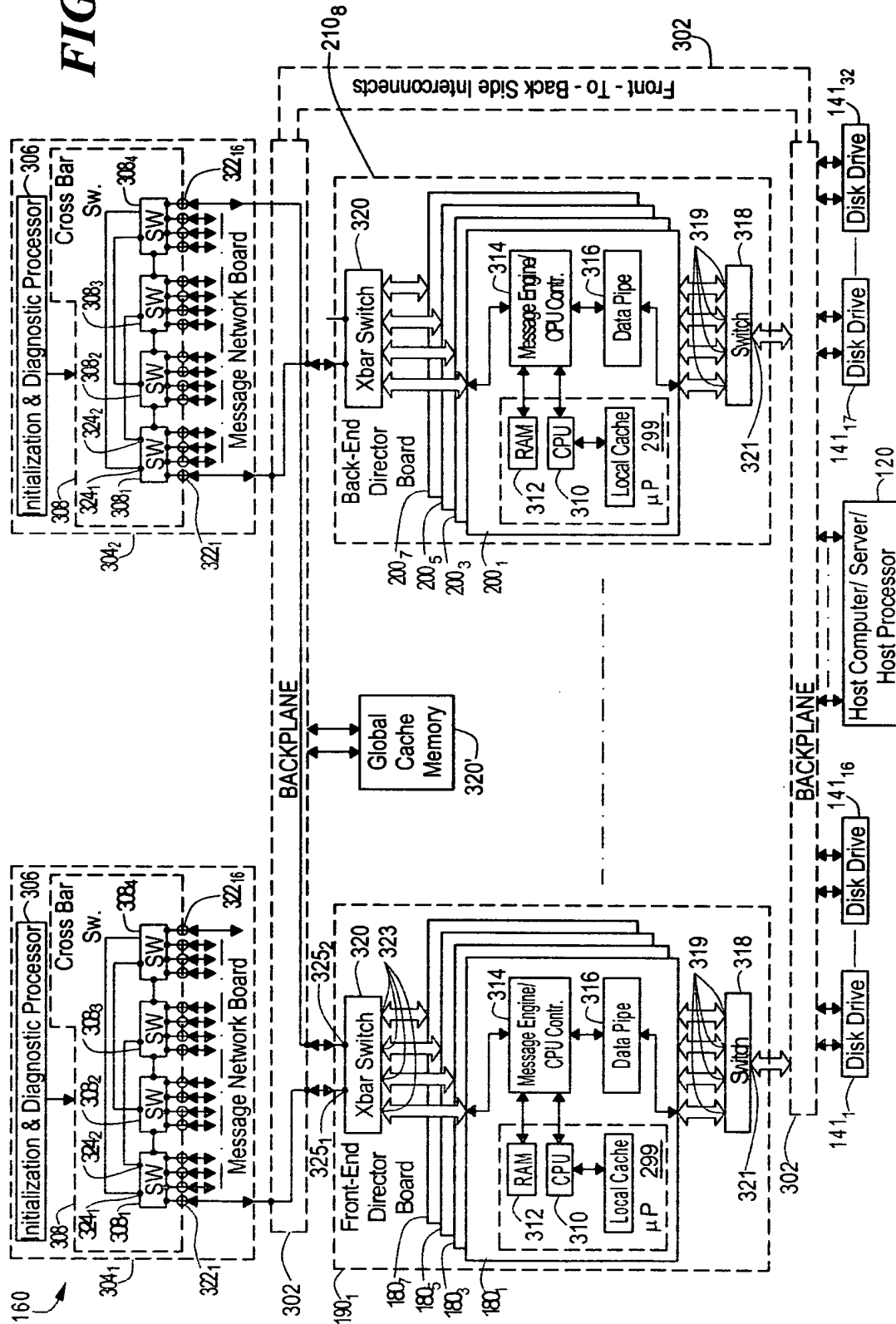
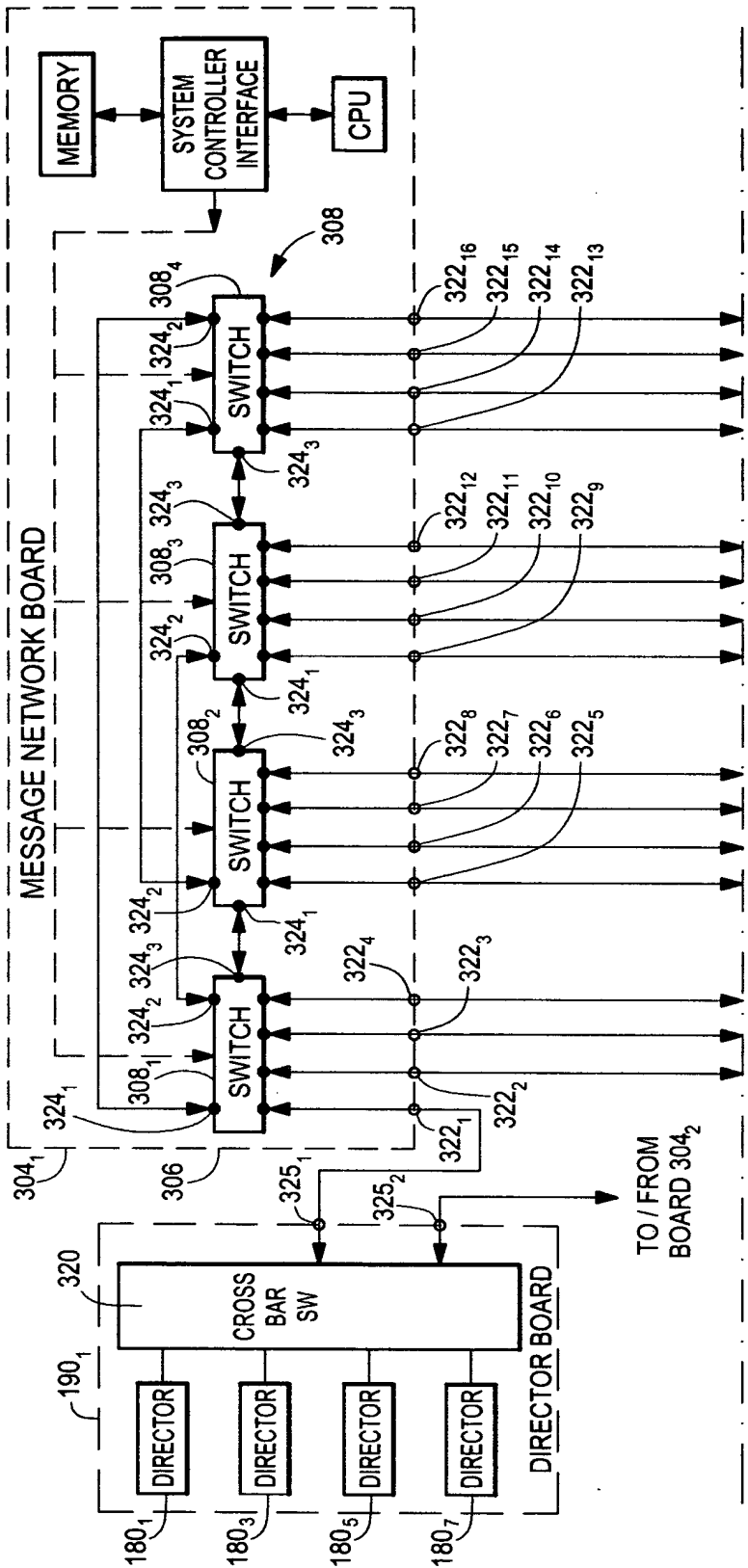




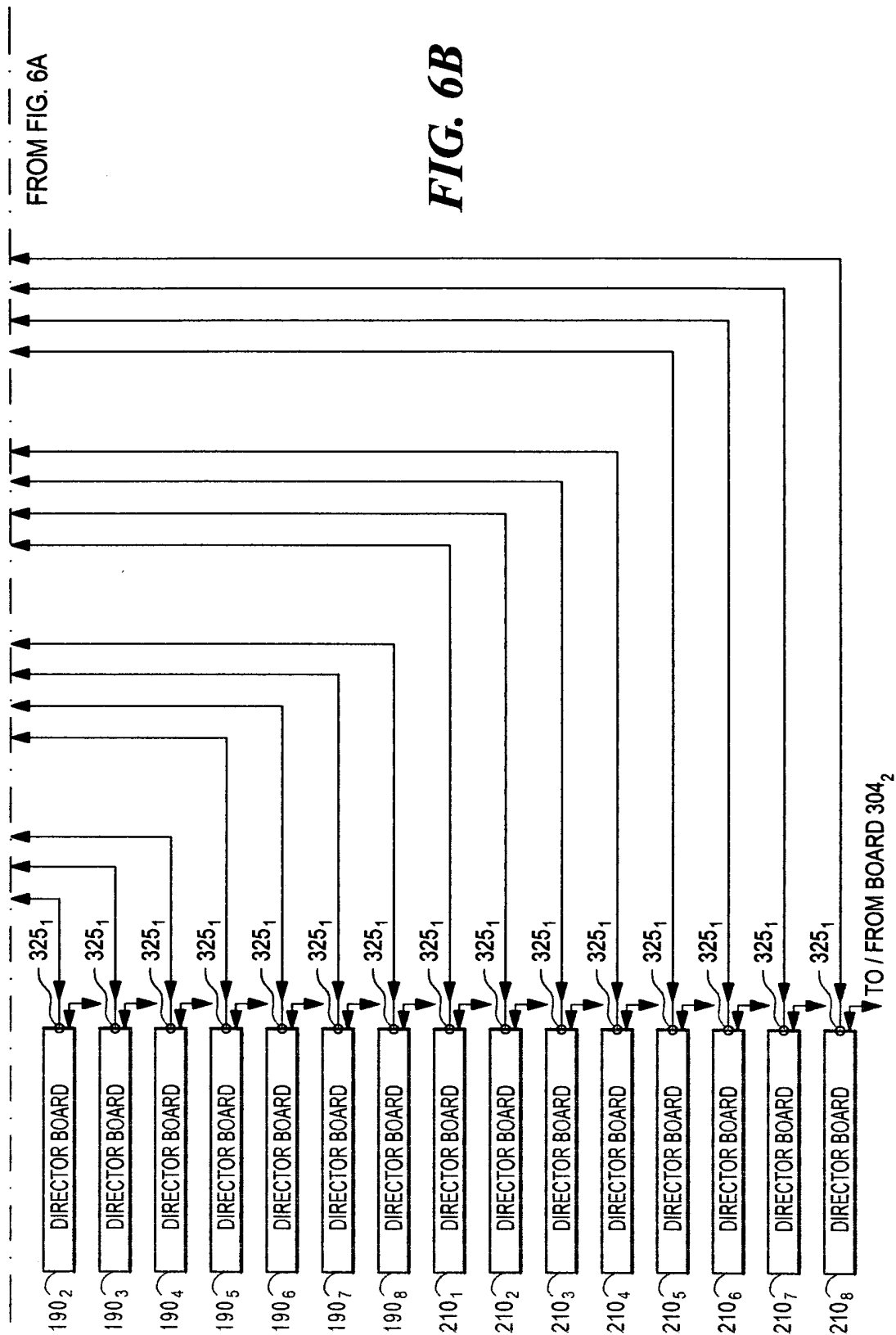
FIG. 6

FIG. 6A
FIG. 6B



TO FIG. 6B

FIG. 6A





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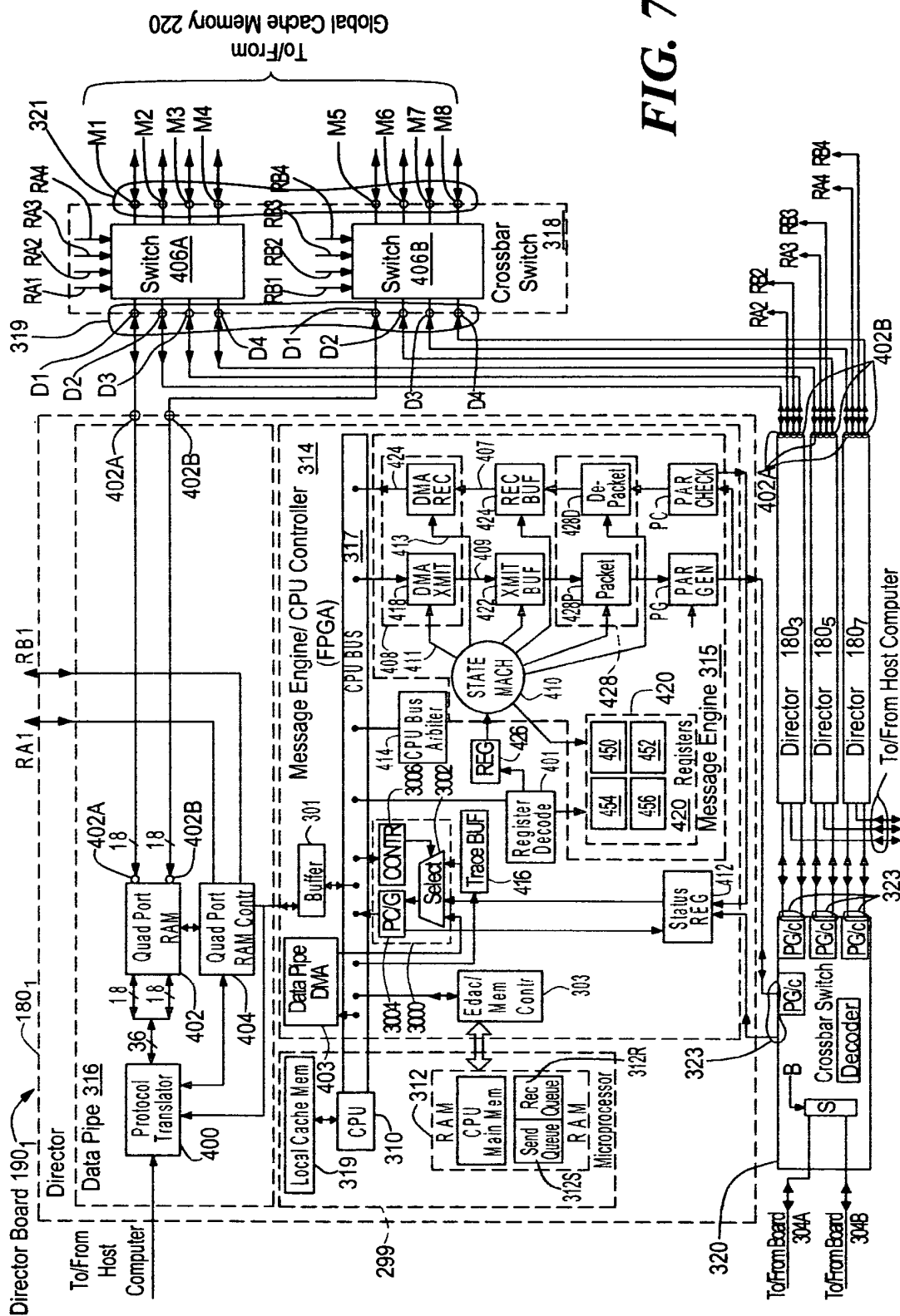


FIG. 7

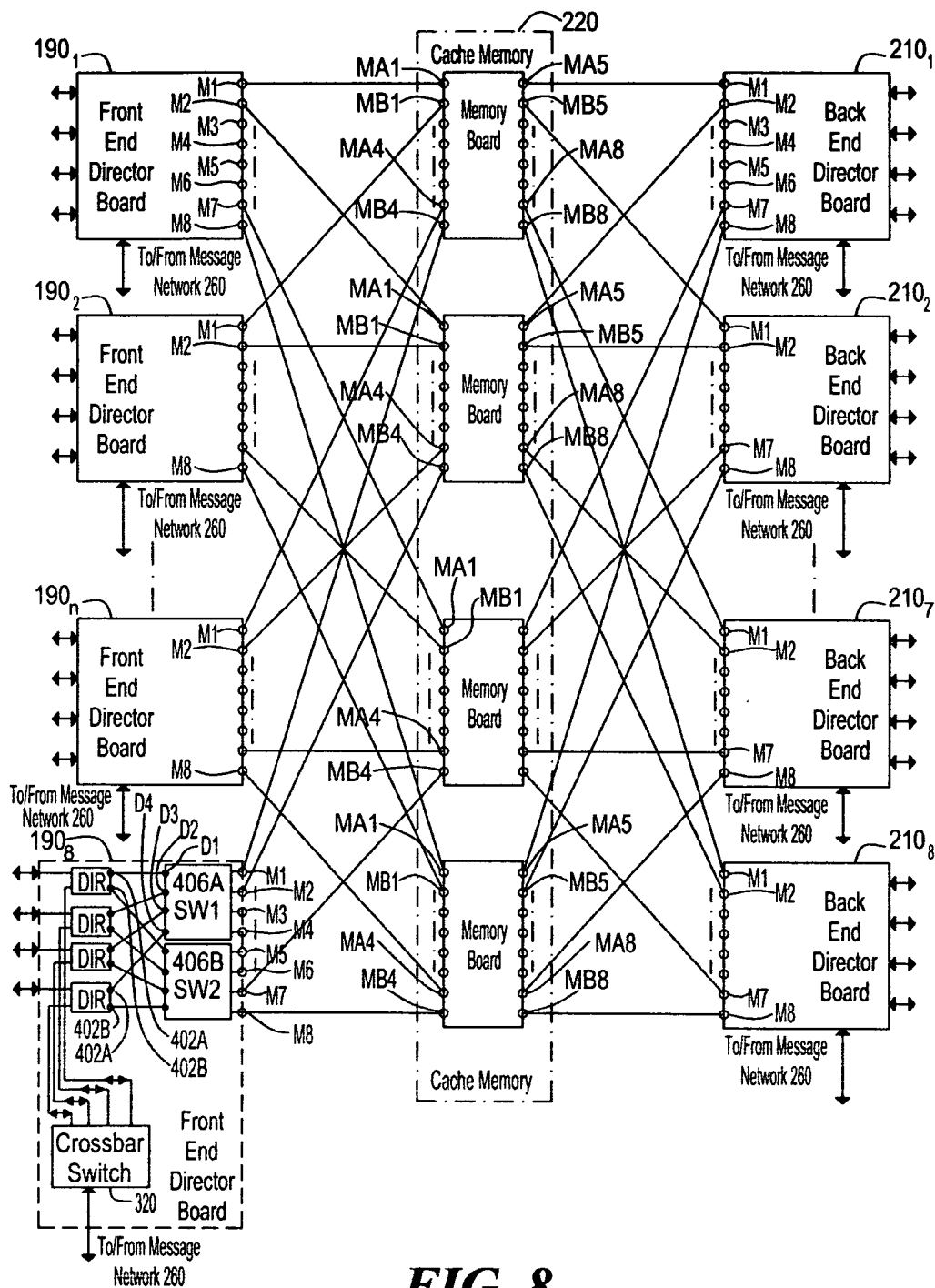
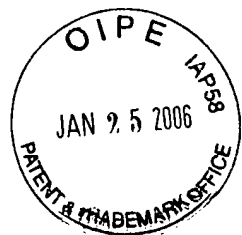


FIG. 8

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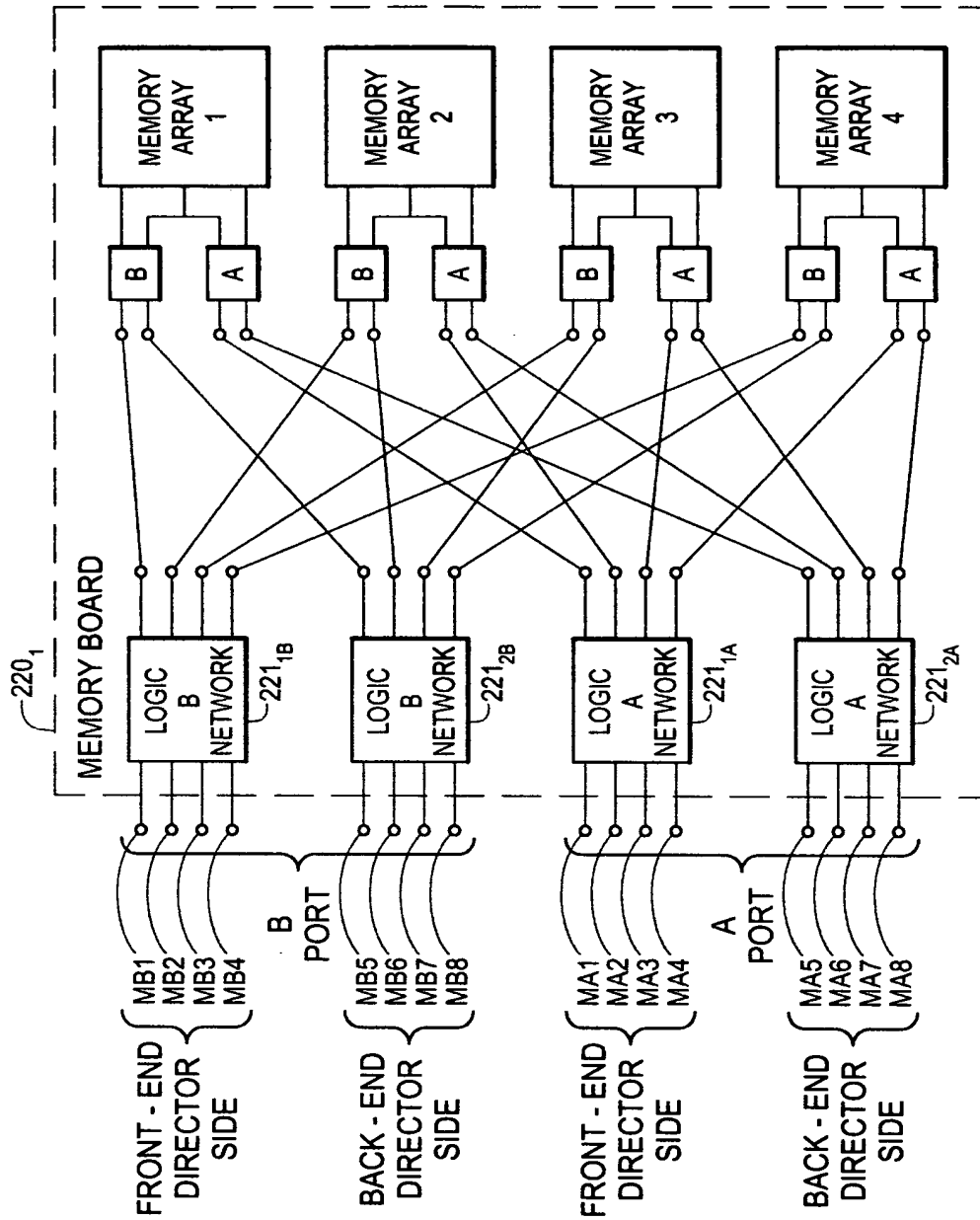


FIG. 8A

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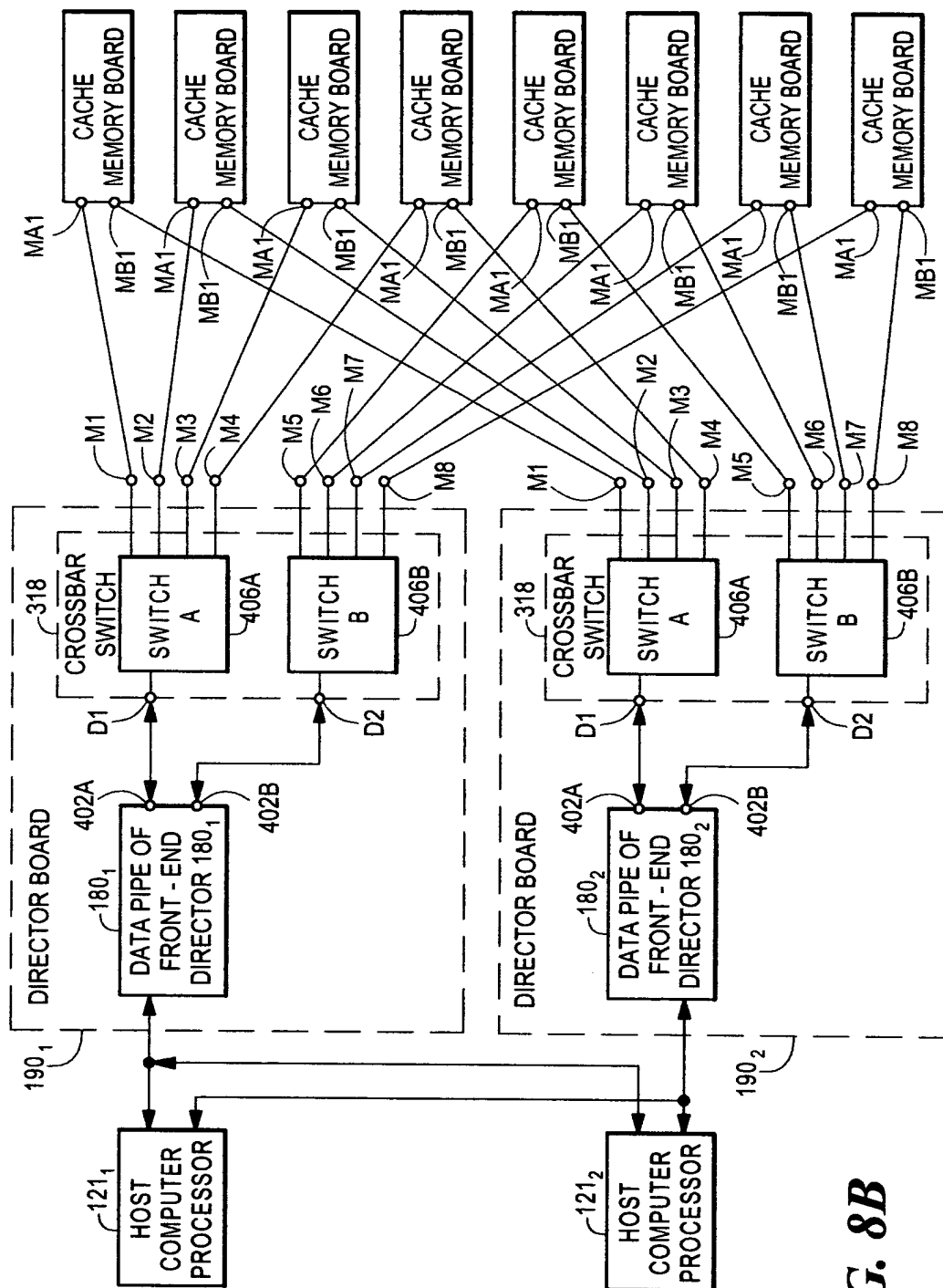


FIG. 8B

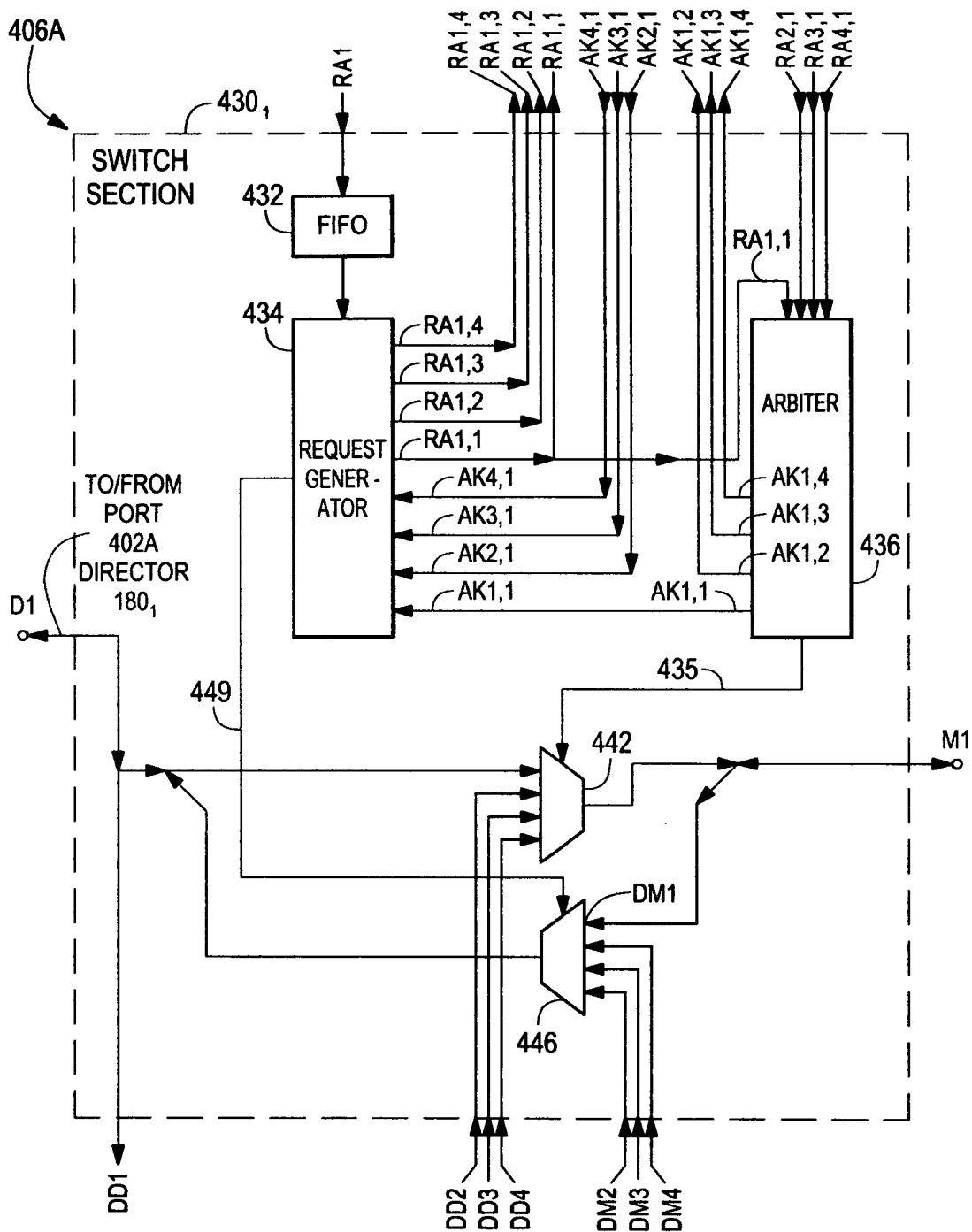


FIG. 8C

FIG. 8C-1

FIG. 8C-2

FIG. 8C-1

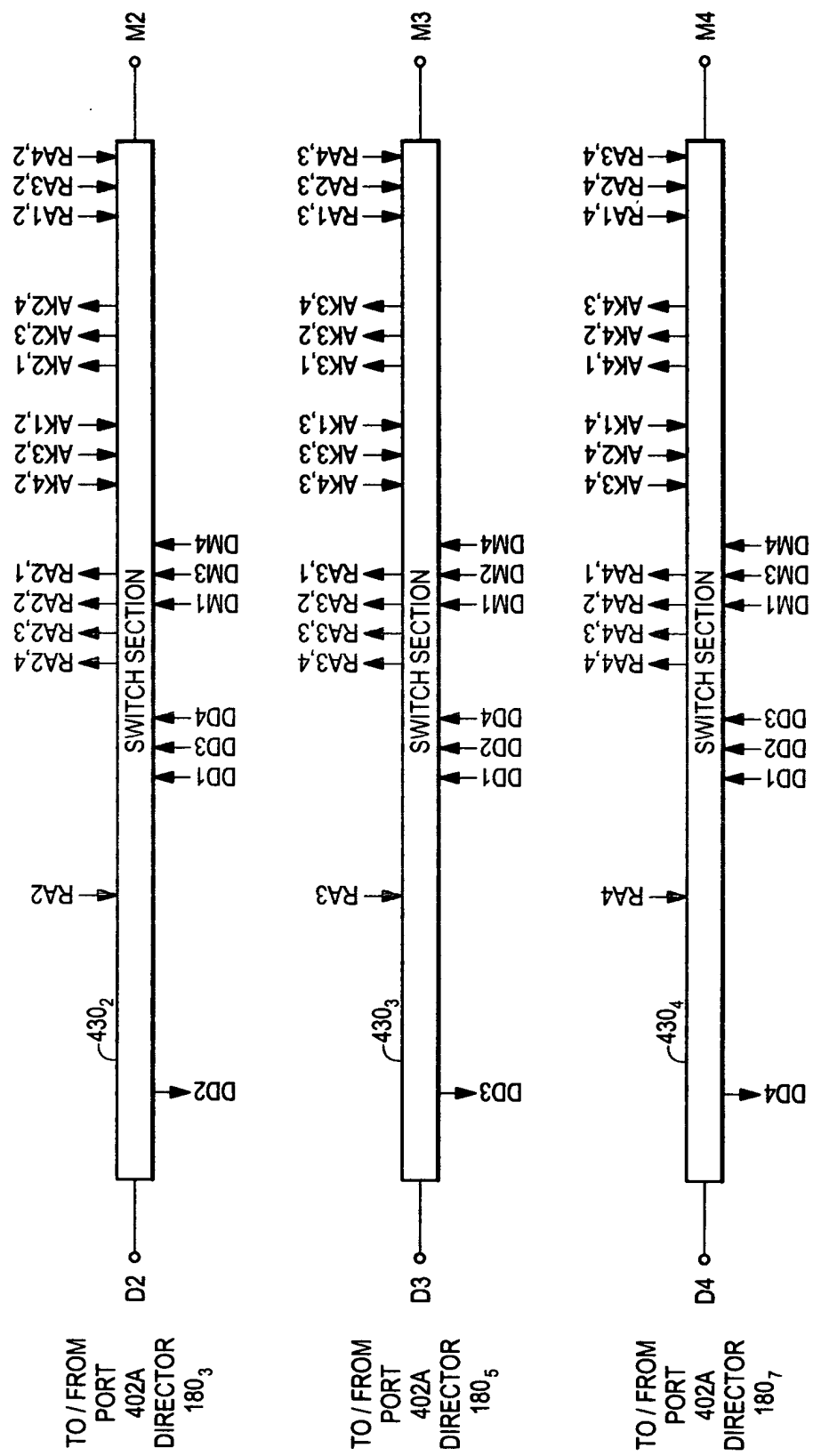
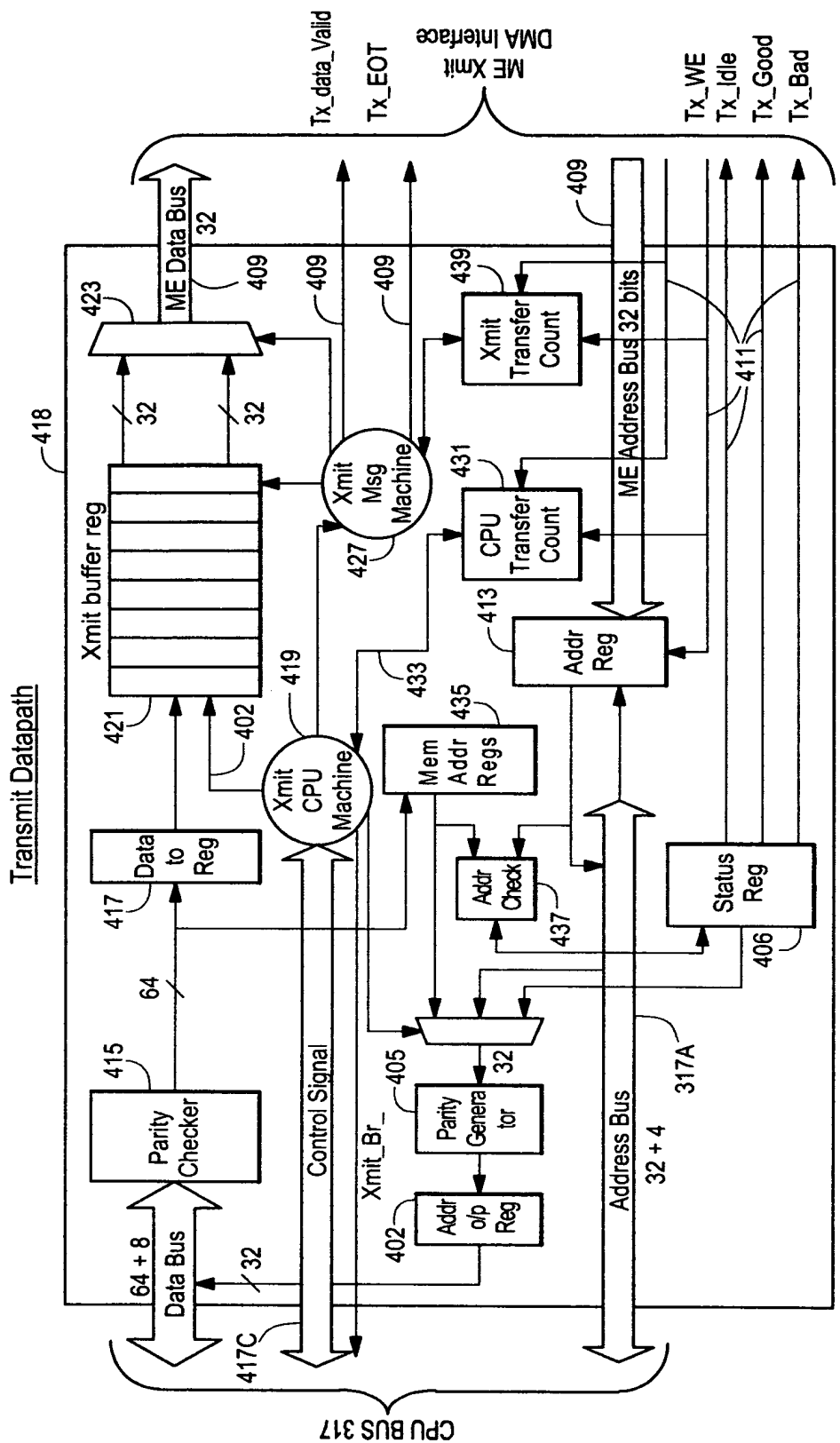


FIG. 8C-2



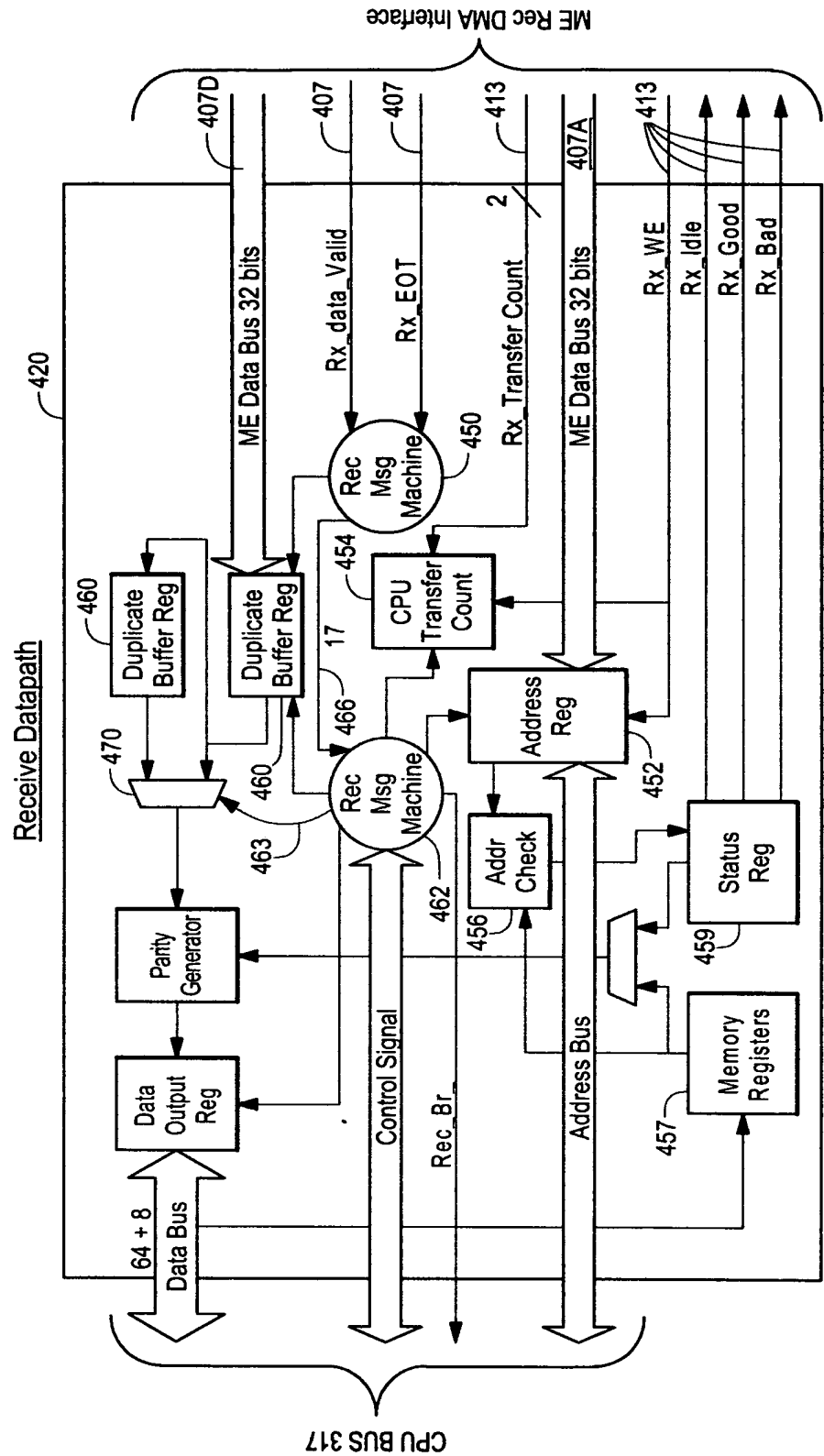


FIG. 10

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FIG. 11A

FIG. 11B

FIG. 11

Message Bus Send Operation

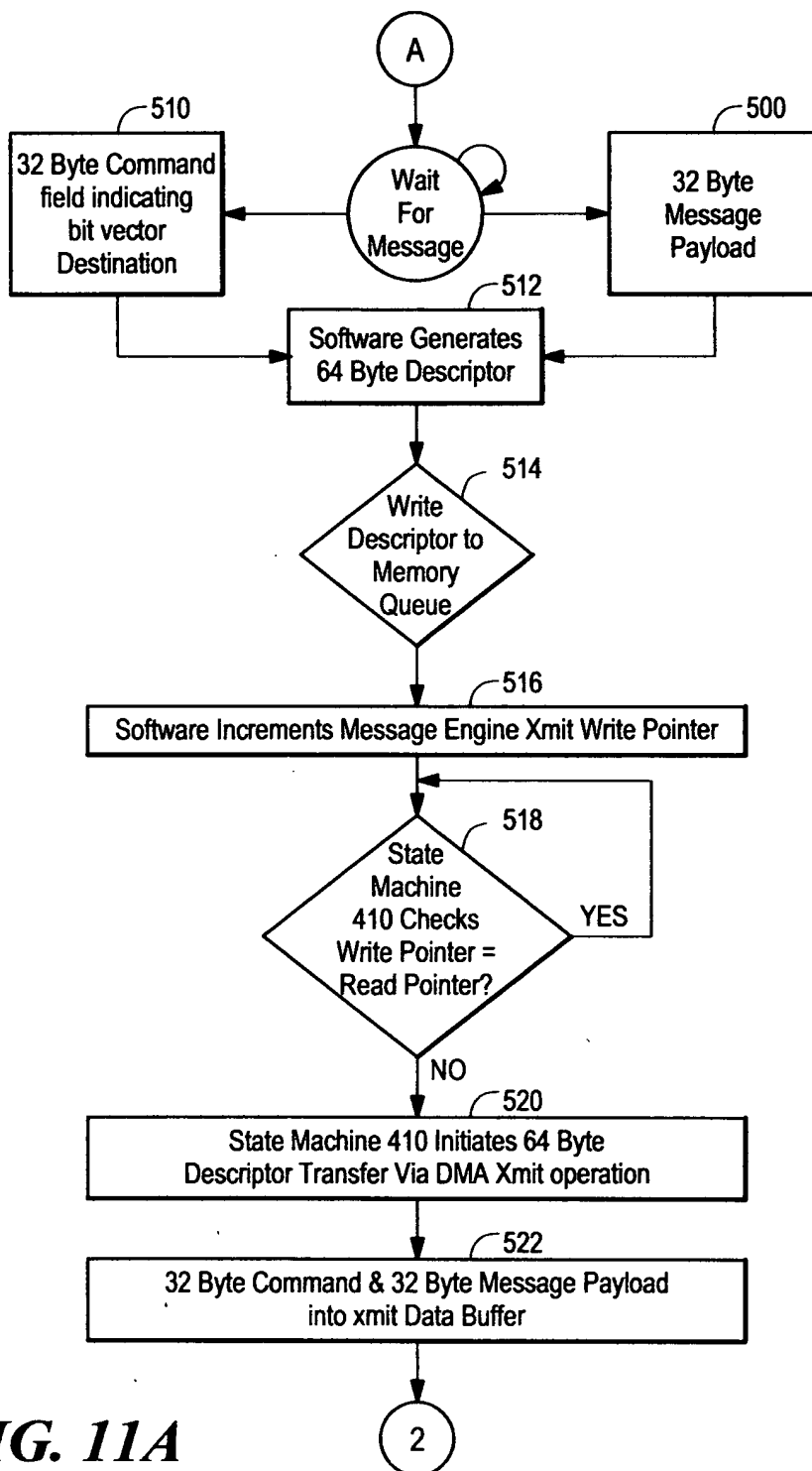


FIG. 11A



Message Bus Send Operation Continued

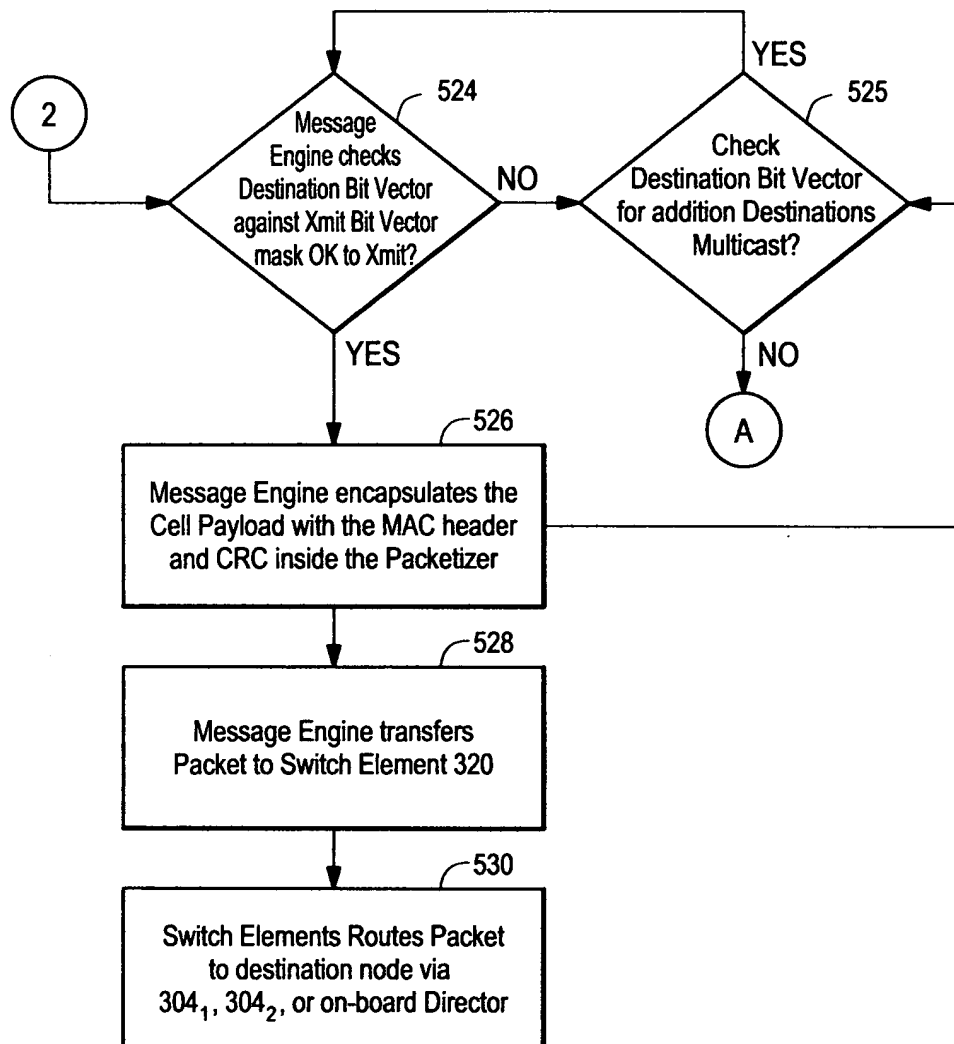
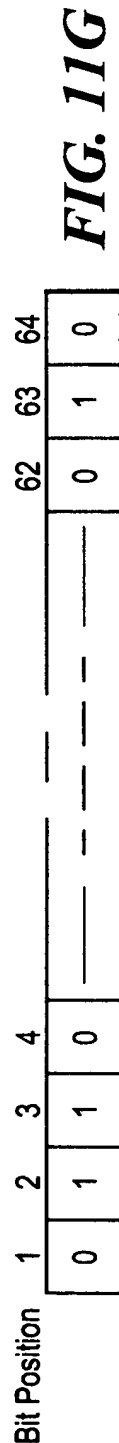
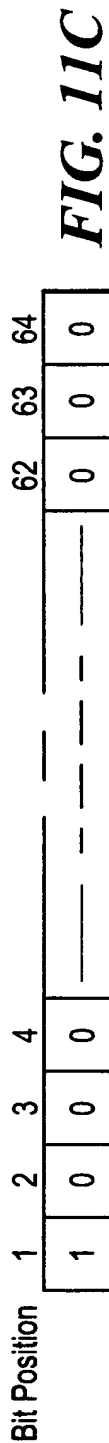


FIG. 11B



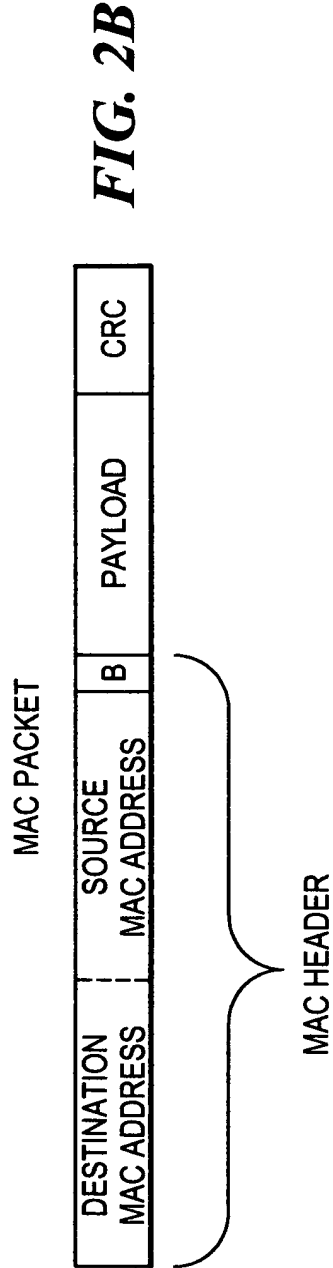
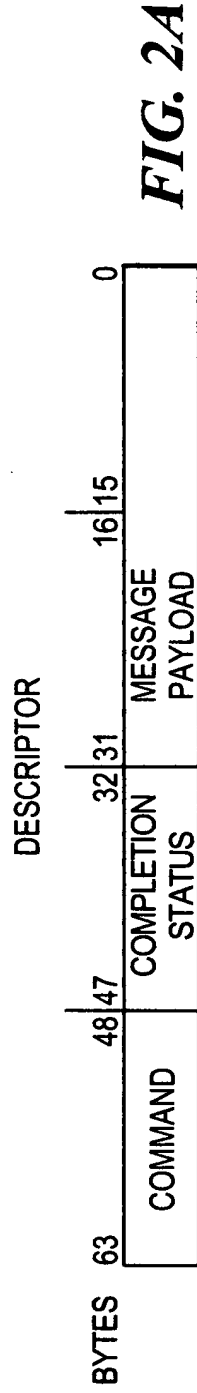




FIG. 12

FIG. 12A

FIG. 12B

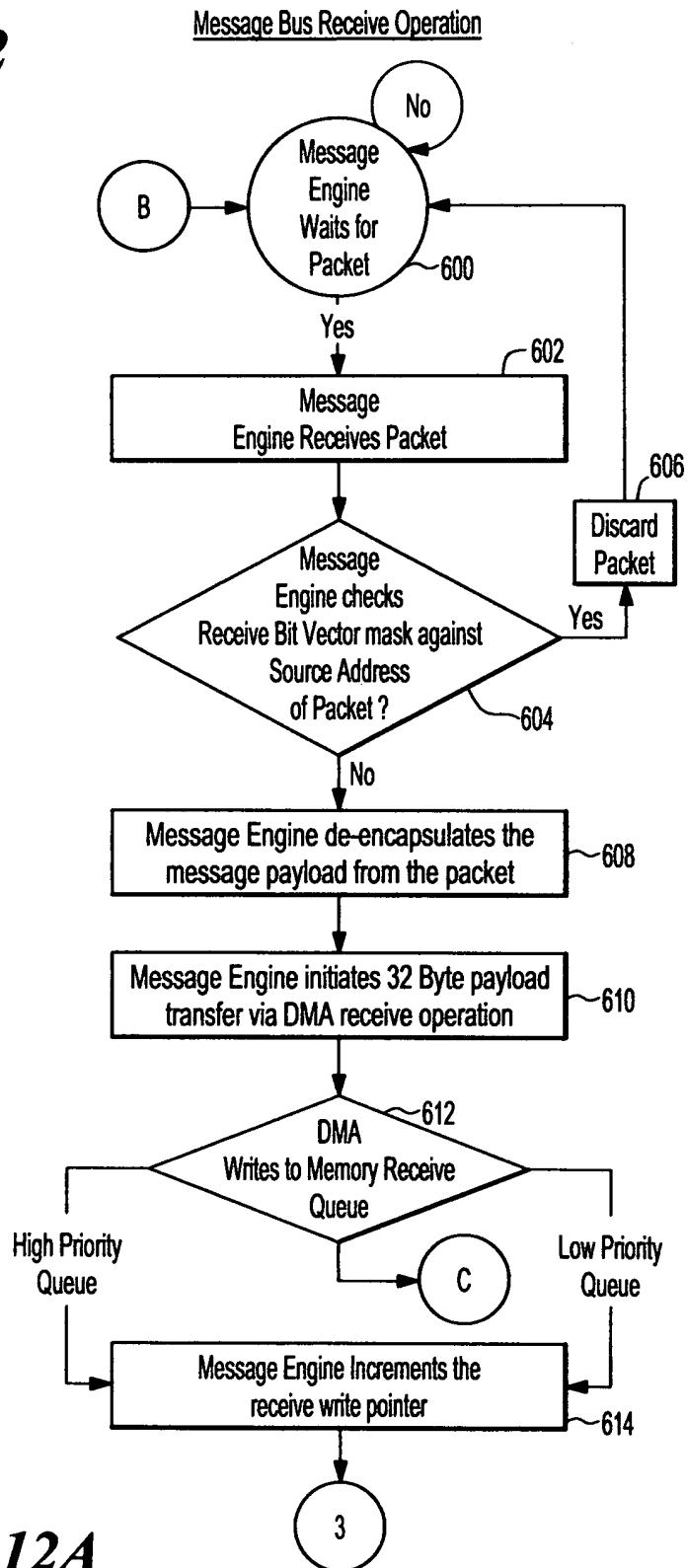


FIG. 12A

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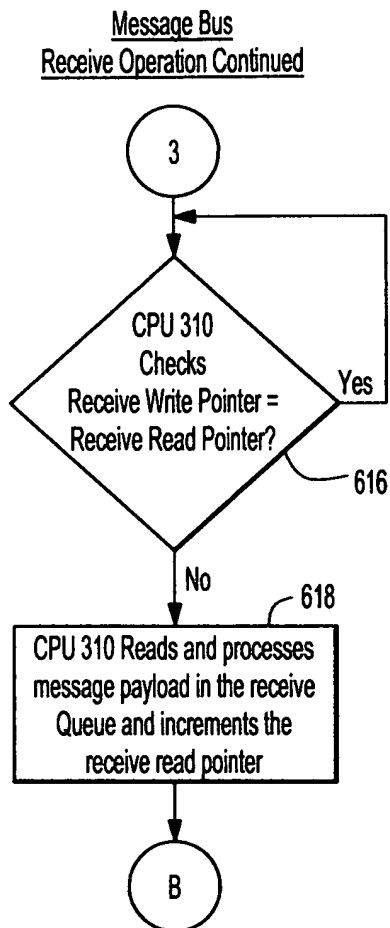


FIG. 12B

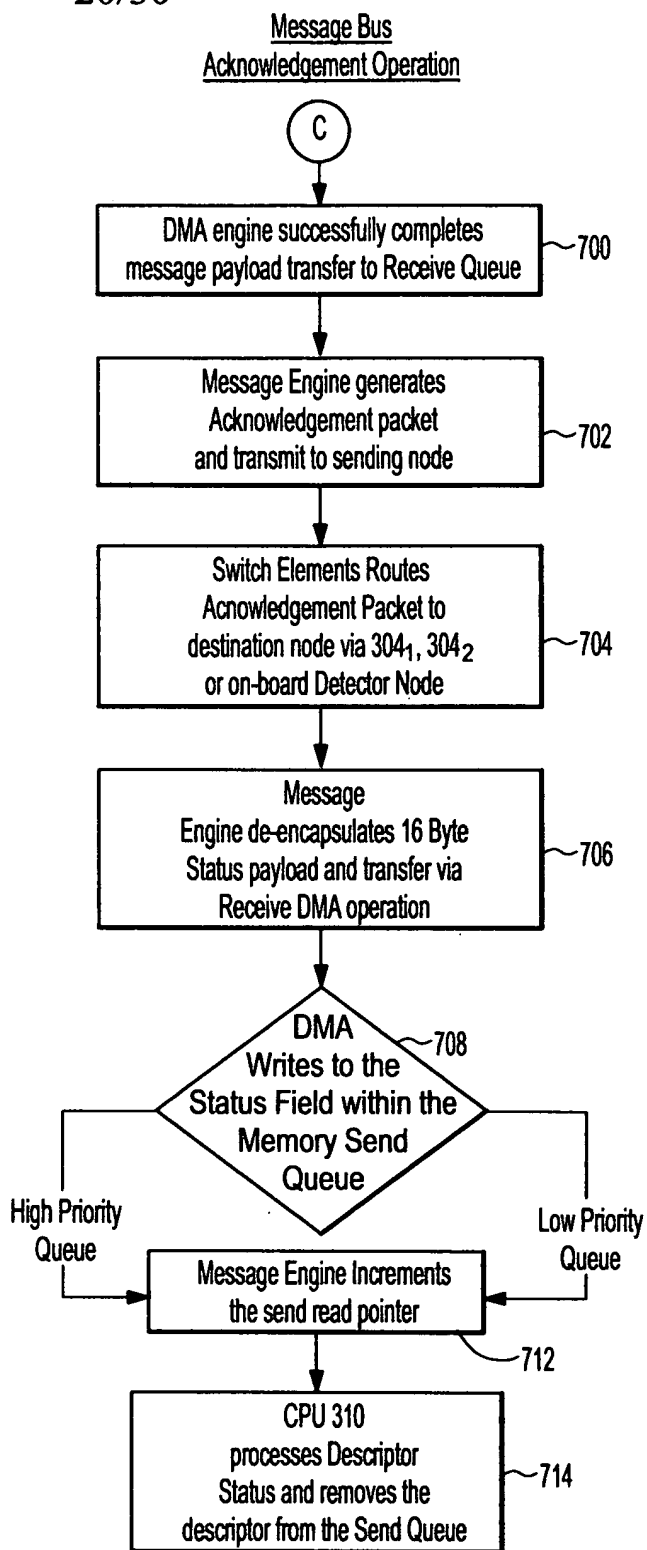


FIG. 13

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Xmit CPU flow

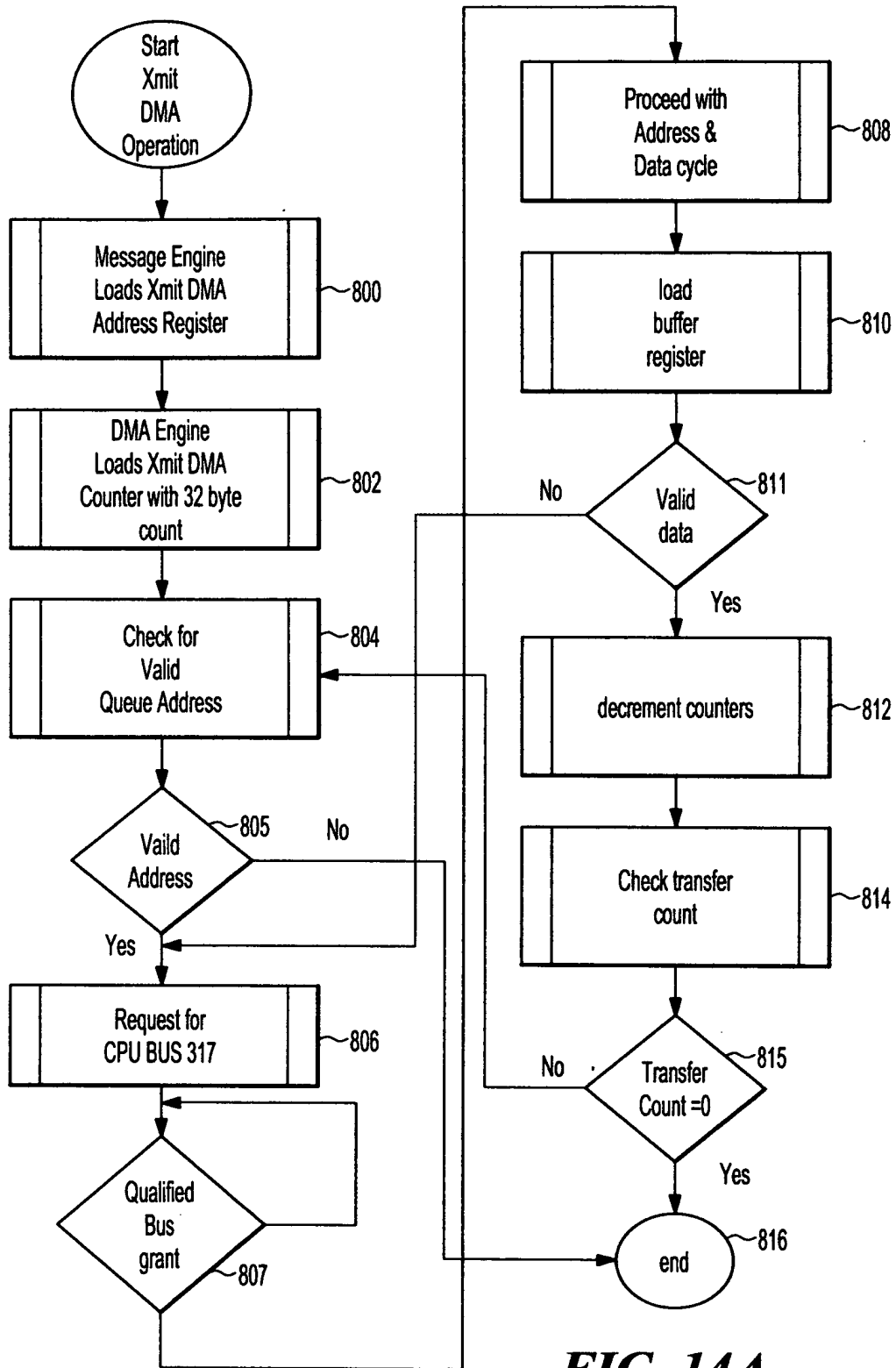
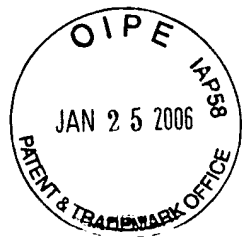


FIG. 14A



Xmit Msg flow

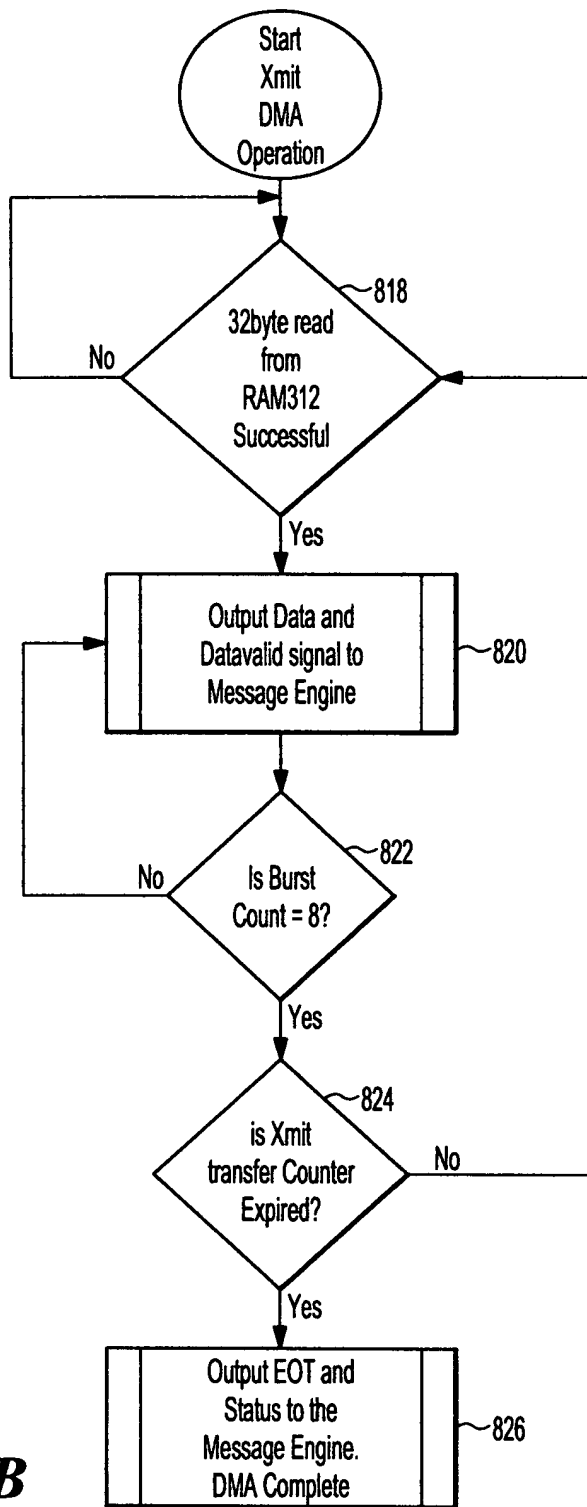


FIG. 14B



Rec msg flow

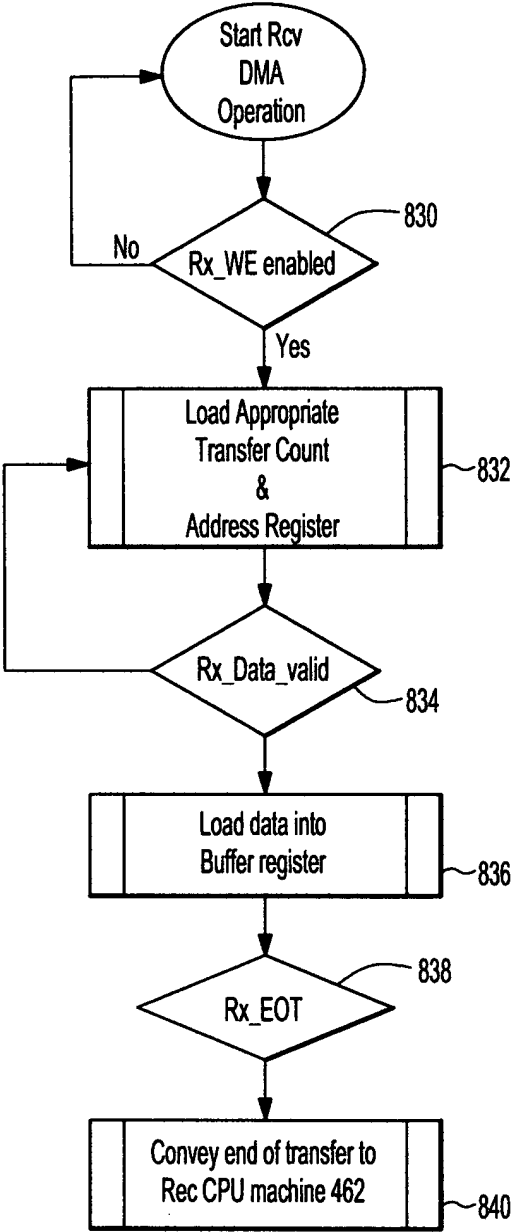


FIG. 15A

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Rec cpu flow

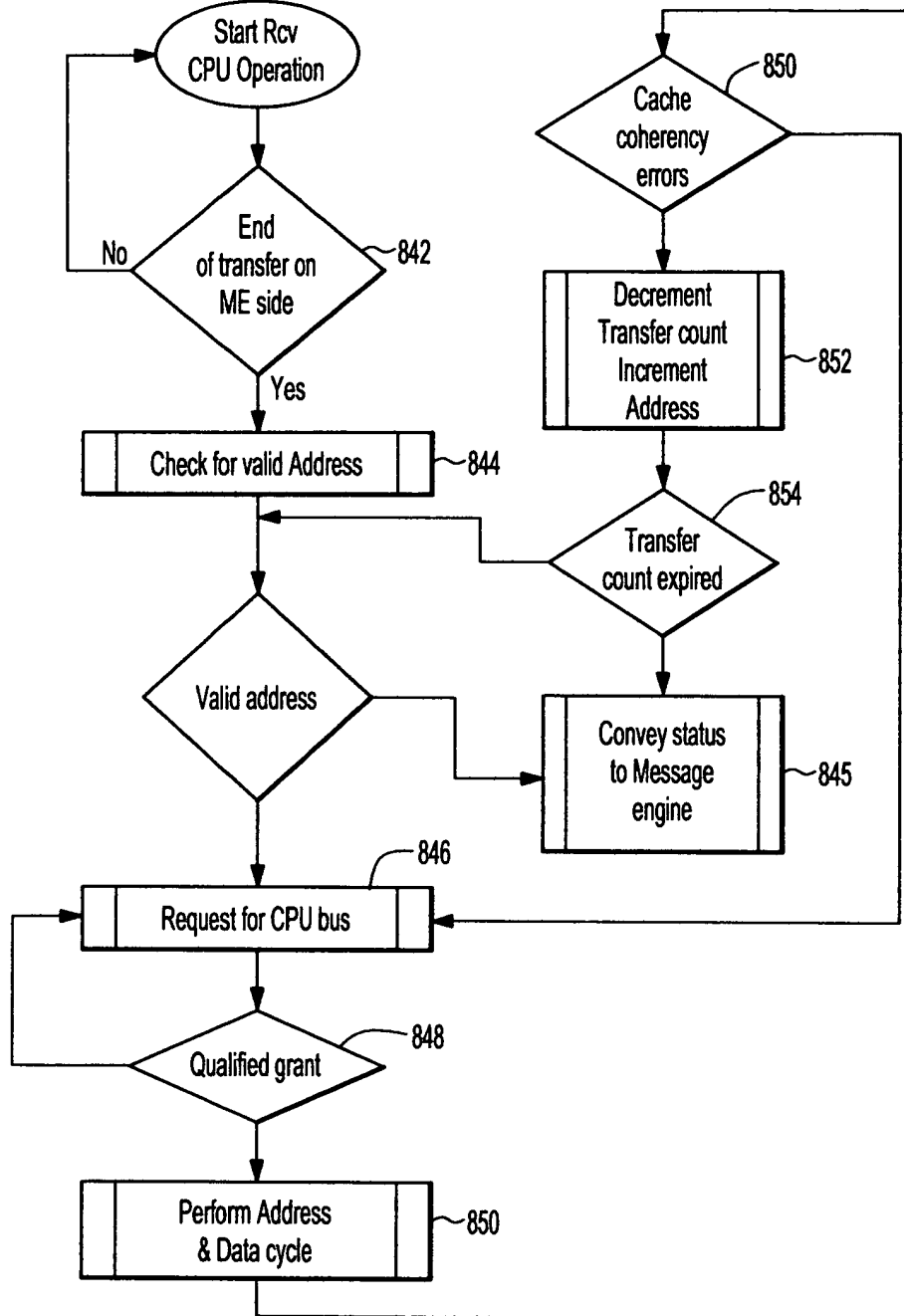


FIG. 15B

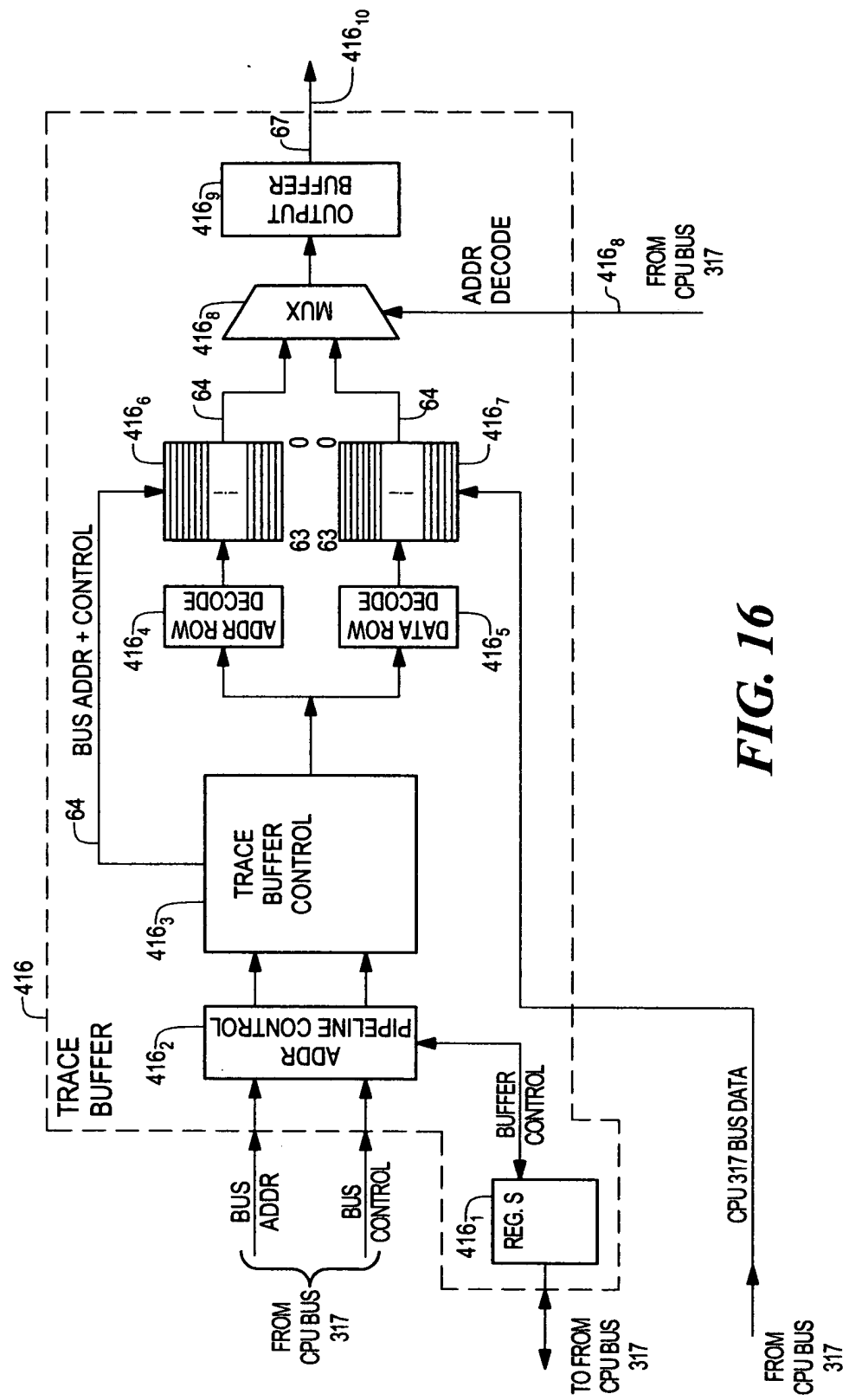


FIG. 16

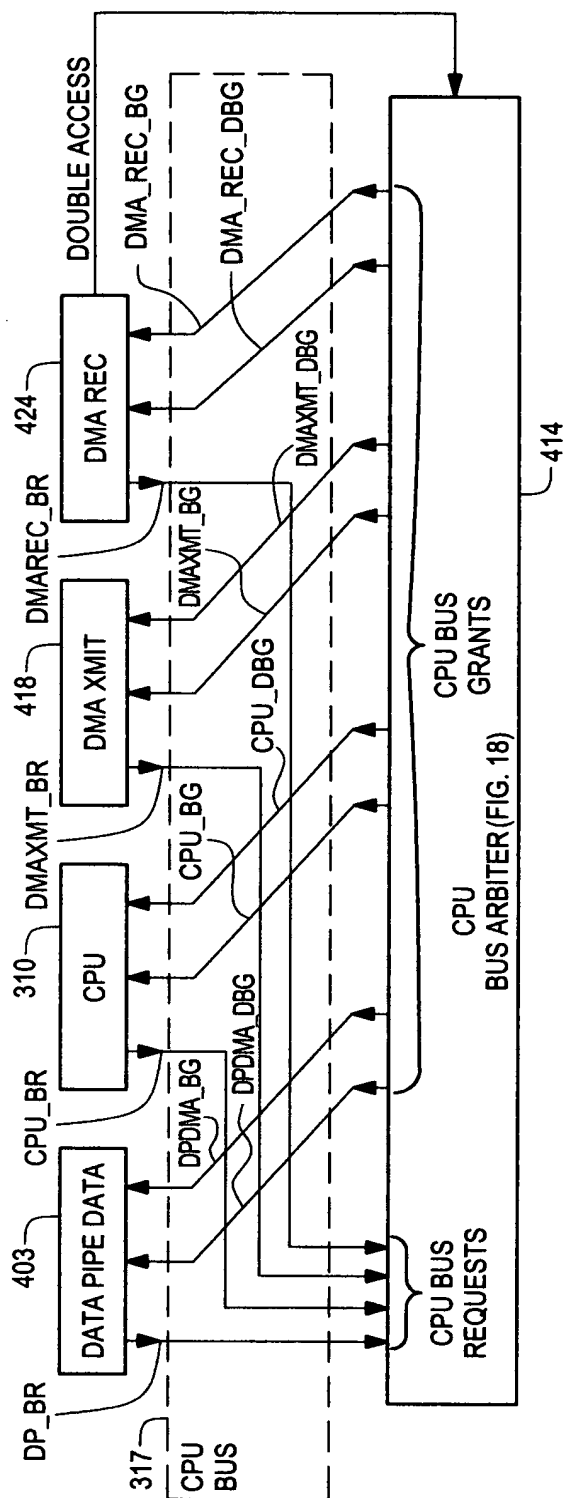
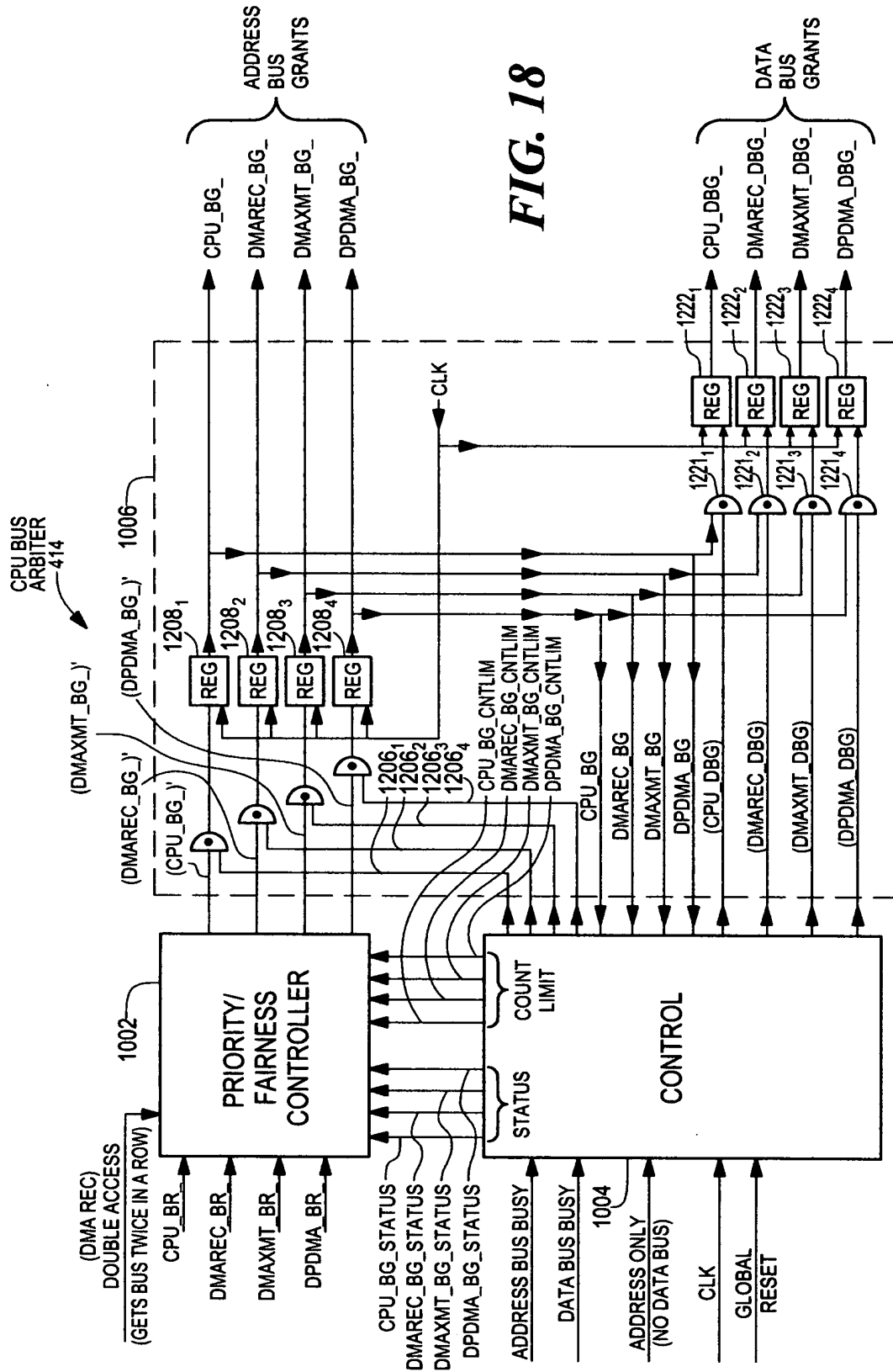


FIG. 17

FIG. 18





POTENTIAL GRANT TO	CPU_ BR	DMAREC_ BR	DMAXMT_ BR	DPDMA_ BR	CPU_BG_ STATUS	DMAREC_BG_ STATUS	DMAXMT_BG_ STATUS	DPDMA_BG_ STATUS	CPU_BG_ CNTLIM	DMAREC_BG_ CNTLIM	DMAXMT_BG_ CNTLIM	DPDMA_BG_ CNTLIM	DOUBLE ACCESS
(CPU_BG')	DC	0	0	0	DC	DC	DC	DC	DC	DC	DC	DC	DC
(CPU_BG')	1	DC	DC	DC	0	DC	DC	DC	DC	0	0	0	0
(CPU_BG')	1	DC	DC	DC	DC	DC	DC	DC	1	DC	DC	DC	0
(DMAREC_BG')	0	1	0	0	DC	DC	DC	DC	DC	DC	DC	DC	DC
(DMAREC_BG')	DC	1	DC	DC	DC	1	DC	DC	DC	DC	DC	DC	1
(DMAREC_BG')	0	1	DC	DC	DC	0	DC	DC	DC	DC	0	0	DC
(DMAREC_BG')	1	1	DC	DC	1	DC	DC	DC	0	DC	0	0	DC
(DMAREC_BG')	DC	1	DC	DC	DC	DC	DC	DC	0	1	DC	DC	DC
(DMAXMT_BG')	0	0	1	0	DC	DC	DC	DC	DC	DC	DC	DC	DC
(DMAXMT_BG')	0	0	1	DC	DC	DC	0	DC	DC	DC	DC	0	DC
(DMAXMT_BG')	0	1	1	DC	DC	1	DC	DC	DC	DC	DC	0	0
(DMAXMT_BG')	1	0	1	DC	1	DC	DC	DC	DC	DC	DC	0	DC
(DMAXMT_BG')	DC	DC	1	DC	DC	DC	DC	DC	0	0	1	DC	0
(DPDMA_BG')	0	0	0	1	DC	DC	DC	DC	DC	DC	DC	DC	DC
(DPDMA_BG')	0	0	1	1	DC	DC	1	0	DC	DC	DC	DC	DC
(DPDMA_BG')	0	1	0	1	DC	1	DC	DC	DC	DC	DC	DC	0
(DPDMA_BG')	1	0	0	1	1	DC	DC	DC	DC	DC	DC	DC	DC
(DPDMA_BG')	DC	DC	DC	1	DC	DC	DC	DC	0	0	0	1	0

FIG. 19

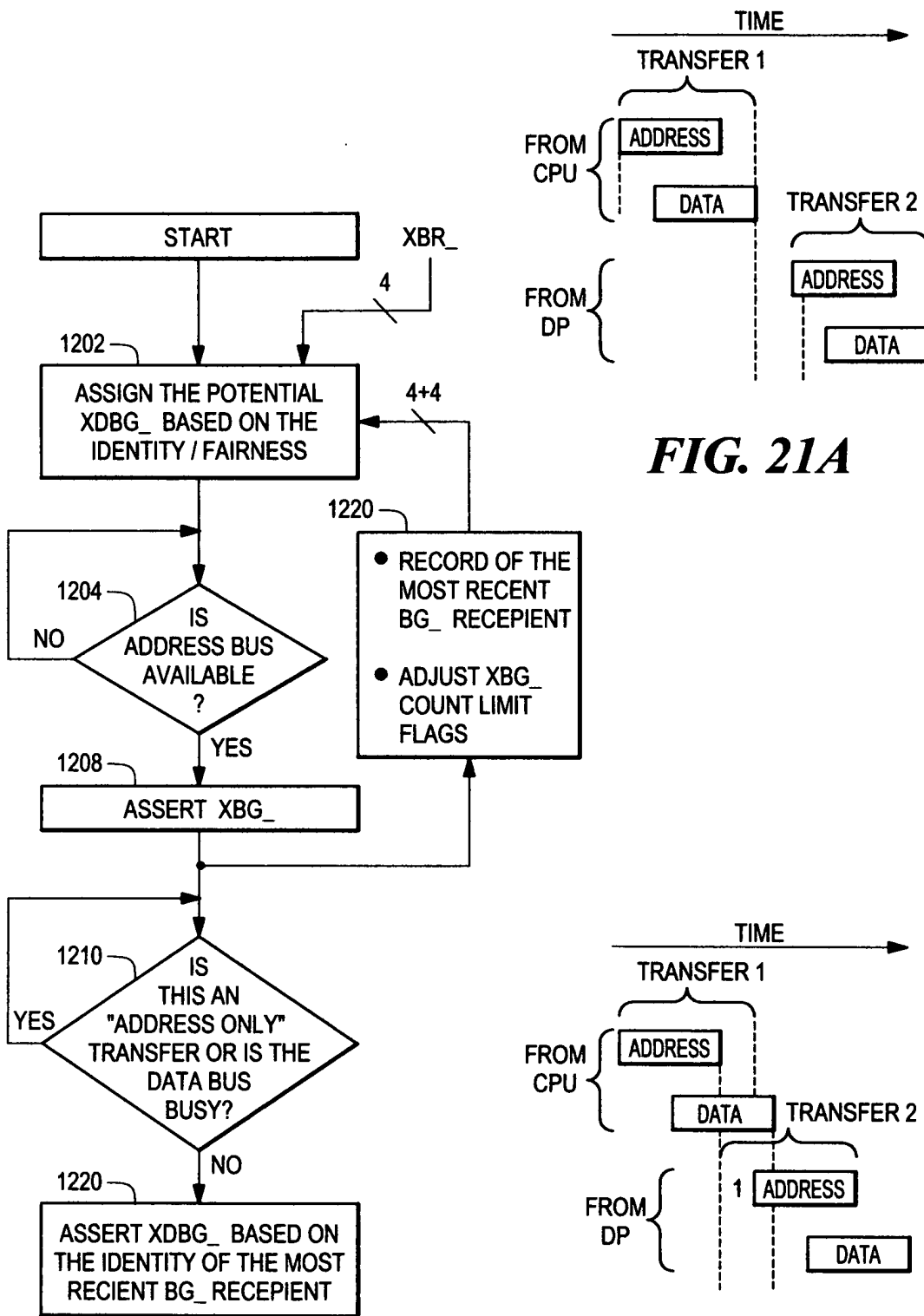


FIG. 20

FIG. 21B

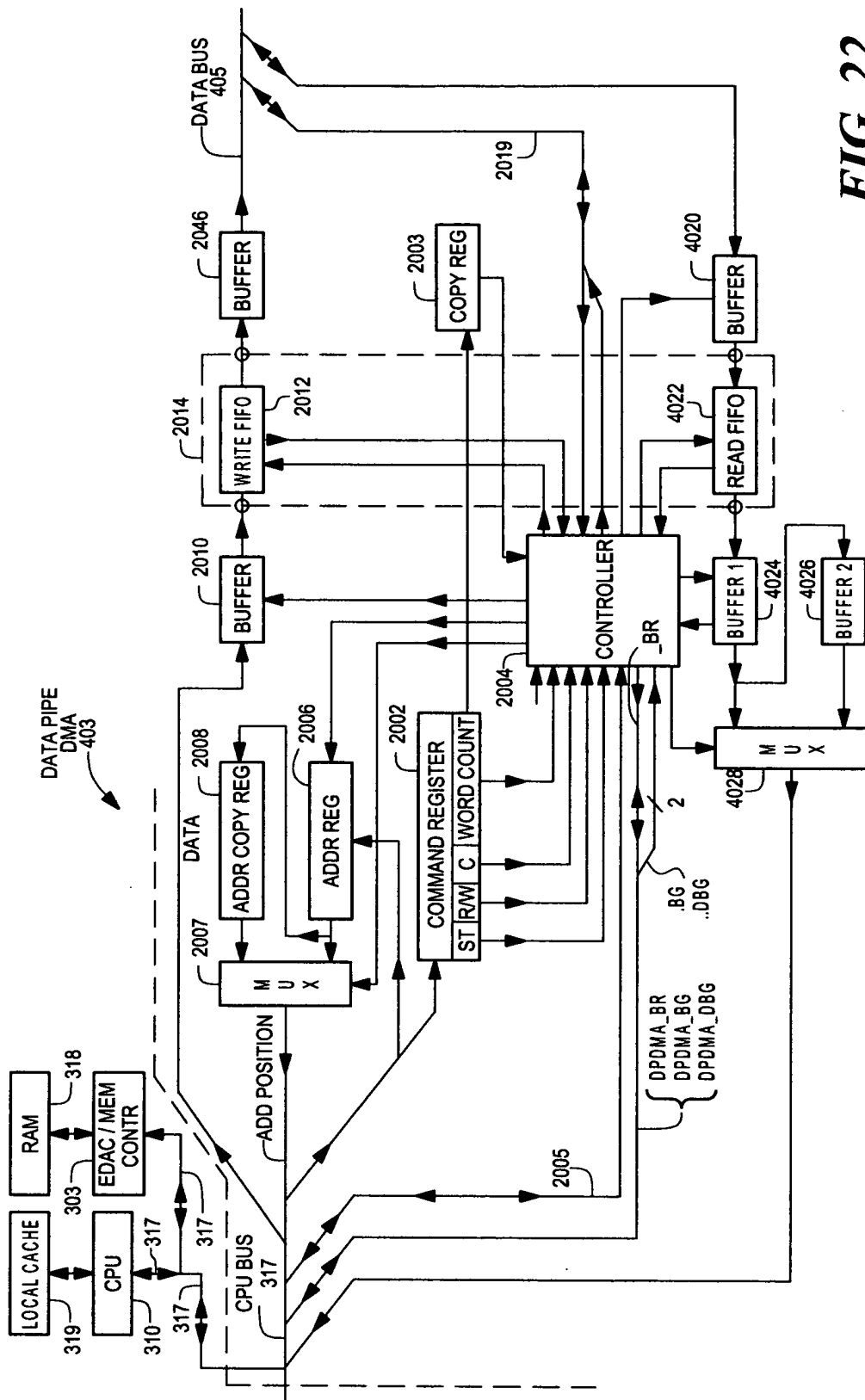


FIG. 22